**MAST**

**HIGH SCALE FUNCTIONAL TEST FOR COMPLEX SOC AND EMBEDDED INSTRUMENT**

**BENEFITS**

- High-scale test of complex SoC:
  - Hundreds of test instruments
  - Custom topologies
  - Dynamic and functional testing
  - Makes dynamic and interactive test for embedded instruments real
  - Functional reuse of test infrastructure
  - Portability between Design, DFT, test and product engineering
  - Support for arbitrary interfaces

**KEYWORDS**

- IEEE 1687-2014, IJTAG
- IEEE 1500, Embedded Core Test
- Embedded Instrumentation
- SoC, DIT, EDA, Debug, Yield Analysis, In-Field Analysis
- Debug, Design For Test (DFT) Yield Analysis, In-Field Analysis

**INTELLECTUAL PROPERTY**

- APP Deposit: 18 June 2015

**LABORATORY**

- TIMA - Grenoble INP

**MATURITÉ TECHNOLOGIQUE & USAGES**

**TRL (Technology readiness level)**

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |

**URL (Usage readiness level)**

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |

**APPLICATIONS**

For actors in all fields of semiconductor design and manufacturing (IP Provider, Design House, Fabless, IDM, Test house).

**CONTEST**

The tests used during and after silicon manufacturing of System-on-Chip (SoC).
Modern SoC uses complex test networks to access embedded instruments (MBIST, LBIST, sensors, configuration,…).

**TECHNOLOGY**

The MAST software is the first solution to support dynamic and interactive tests for SoC embedded instruments.
MAST is a protocol aware environment which allows development of complex test algorithms at IP level, and automatically performs execution at SoC level.
The solutions is based on the new IEEE 1687-2014 (IJTAG), supports IEEE 1500 (Embedded Core Test), and also custom ad-hoc networks. It supports several physical interfaces for chip access, like for instance JTAG, I2C or SPI.
MAST can be run standalone with high level models. It can interface directly with an HDL simulator or an emulation board. Finally, it can also run directly on the ATE.
Compared to existing commercial solution which only focus on pre-generated static test (e.g. ATPG tests), MAST works on true dynamic and interactive tests.

**ADVANTAGES**

MAST provides an answer to two recurring problems faced by semiconductor companies:
- Limitation in test definition: MAST provides an interface to build elaborate and dynamic tests vectors which adapts to Design-Under-Test (DUT) behavior. These algorithms can run massively, in parallel, and access the instruments around IPs in a minimum run-time.
- Waste of resources on tedious manual tasks: MAST allows reuse and automation at each phase of a product lifecycle by using standard models and languages. It guarantees the portability of test definition and execution from the design to the final deployment and usage.
Makes dynamic test for embedded instruments real. Unifies the flow and methodology from high level RTL DFT down to bench and ATE. Faster ATE bring-up with "protocol aware" interactive environment.

**MATURITY**

The software works under Linux, Windows and Embedded Linux using standard libraries. Validation and testing have been done on a representative set of examples in emulation, simulation and prototyping.

**PROJECT**

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